## REMARKS

The Official Action mailed January 26, 2007, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on August 28, 2003; December 3, 2004; October 17, 2005; December 9, 2005; April 24, 2006; and October 31, 2006.

Claims 3-5, 8, 13, 18, 23, 28, 33, 36-43, 45, 47-57 and 74-80 were pending in the present application prior to the above amendment. Claims 3, 4 and 74 have been amended to correct minor informalities, and new dependent claim 81 has been added to recite additional protection to which the Applicant is entitled. Accordingly, claims 3-5, 8, 13, 18, 23, 28, 33, 36-43, 45, 47-57 and 74-81 are now pending in the present application, of which claims 3, 36, 37 and 74 are independent. The Applicant notes with appreciation the allowance of claims 36-43, 45 and 47-57 (page 6, Paper No. 20070117). For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

The Official Action rejects claims 3-5, 8, 13, 28, 33, 74, 76-77, 79-80 as obvious based on the combination of U.S. Patent Application Publication No. 2002/0056839 to Joo and U.S. Patent Application Publication No. 2001/0049163 to Yamazaki. The Applicant respectfully traverses the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim

limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The prior art, either alone or in combination, does not teach or suggest all the features of the independent claims. Independent claim 3 recites that a conductive layer extends beyond each periphery of first and second semiconductor layers at least when selective heating of the first and second semiconductor layers is performed. Independent claim 74 recites that a conductive layer extends beyond each periphery of the a semiconductor layer at least when the selective heating of the semiconductor layer is performed. Dependent claim 4 recites a step of etching the conductive layer after the selective heating of the first and second semiconductor layers to form at least first and second gate electrodes over the first and second semiconductor islands, respectively. New dependent claim 81 recites a step of etching the conductive layer after the selective heating of the semiconductor layer to form a gate electrode over the semiconductor layer.

In the present invention, when selective heating is performed, a region in the substrate where the conductive layer is formed and another region inevitably differ from each other in temperature. Thus, a thermal stress concentrates on a boundary portion therebetween. Since independent claims 3 and 74 include the above-referenced features, the first and second semiconductor layers (or the semiconductor layer) are not

thermally stressed (see, e.g., page 24, line 23, to page 25, line 6; and Figures 1A and 1B, which are reproduced and annotated below).

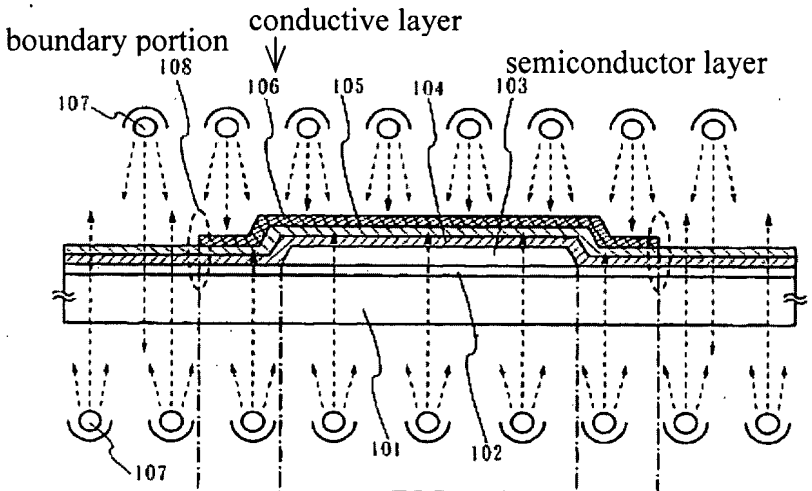



FIG. 1A

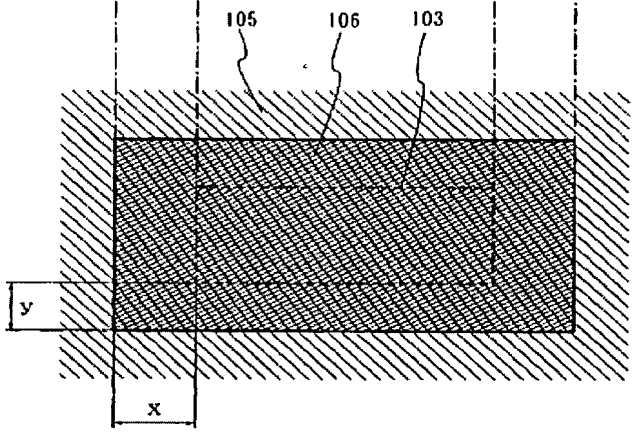
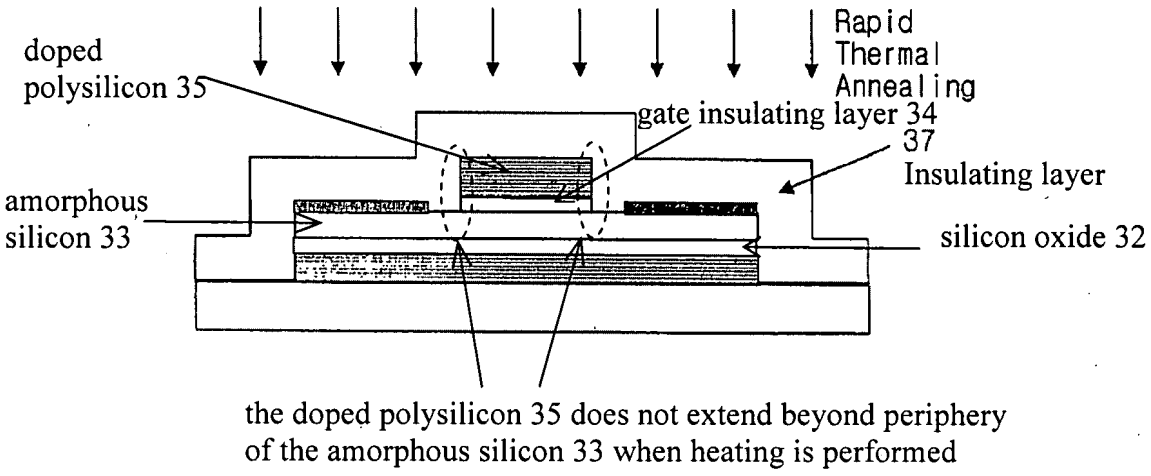



FIG. 1B

The Official Action asserts that Joo teaches "[s]electively heating the first and second semiconductor layer by irradiating an incoherent electromagnetic wave within a wavelength band ranging at least from a visible light band to an infrared band to thereby conducting heat treatment on each of the first and second semiconductor layers and the insulating layer, wherein said conductive layer extends beyond each periphery of the first and second semiconductor layers at least when the selective heating of the first and second semiconductor layers is performed (see paragraphs# 32, figure 3f)" (page 3,

lines 9-14, Paper No. 20070117). A similar assertion is made with respect to claim 74 at page 4, lines 4-8). The Applicant respectfully disagrees and traverses the assertions in the Official Action.

Joo does not teach or suggest the above-referenced features. Joo appears to disclose a manufacturing method of a semiconductor device comprising forming an amorphous silicon 33 over a substrate having a silicon oxide 32, where the amorphous silicon includes a region to become at least a channel region of a thin film transistor (paragraphs [0025]-[0026], Figure 3A); forming a doped polysilicon 35 covering an entire surface of the amorphous silicon with a gate insulating layer 34 interposed therebetween (paragraph [0028], Figure 3B); etching the doped polysilicon and the gate insulating layer (paragraph [0029], Figure 3C); doping source and drain regions (paragraph [0031], Figure 3D); forming an insulating layer 37 (paragraph [0032], Figure 3F); and heating the insulating layer 37 to thereby crystallize the amorphous silicon 33 (paragraphs [0032], Figure 3F), where the doped polysilicon 35 does not extend beyond a periphery of the amorphous silicon 33 when the heating is performed (see Figure 3F, reproduced and annotated below).




In other words, when the semiconductor layer 33 is heated (in Figure 3F), the conductive layer (doped polysilicon 35) does not extend beyond the periphery of the semiconductor layer 33.

Yamazaki '163 does not cure the deficiencies in Joo. The Official Action asserts that Yamazaki '163 teaches "etching the conductive layer after the selective heating the first and second semiconductor layers to form at least first and second gate electrodes over the first and second semiconductor islands, respectively (see figures 2a, 16, meeting clams 3, 4, 74)" (page 4, lines 10-12, Paper No. 20070117). The Applicant respectfully disagrees and traverses the assertions in the Official Action.

Yamazaki '163 discloses the following: "In particular, [the present invention] relates to the constitution of thin film transistors (hereinafter referred to as TFT) having an inverse stagger structure" (paragraph [0001]). Furthermore Yamazaki '163 teaches a manufacturing method of an inverse-staggered type TFT comprising forming a gate electrode over an substrate (paragraphs [0119]-[0120], Figure 1A); forming an insulating layer on the gate electrode (paragraphs [0121]-[0123], Figure 1A); and forming a semiconductor layer over the insulating layer (paragraphs [0124]-[0126], Figure 1A). Figures 2A and 16 are reproduced and annotated below.

FIG. 2A

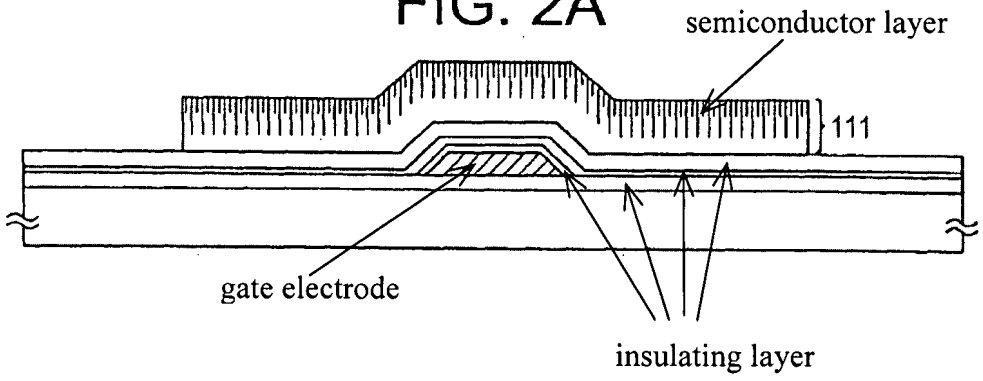
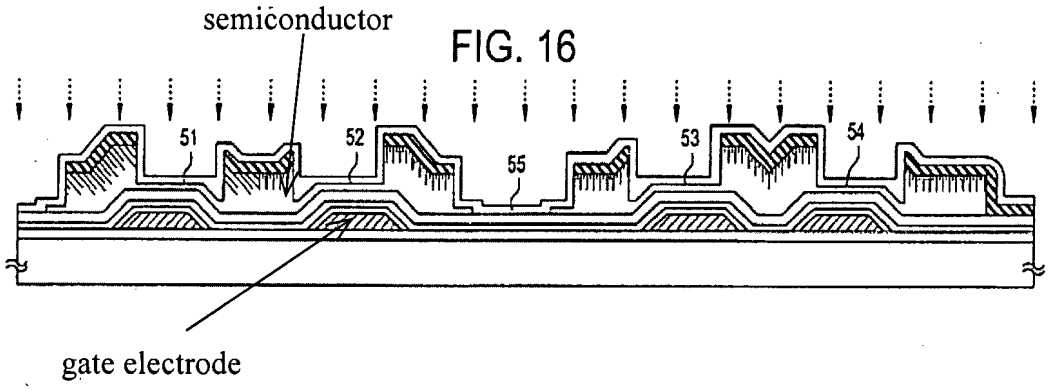


FIG. 16




As such, Yamazaki '163 does not teach or suggest a step of etching the conductive layer after the selective heating of the first and second semiconductor layers (the semiconductor layer) to form at least first and second gate electrodes (a gate electrode) over the first and second semiconductor islands, respectively (the semiconductor layer).

Therefore, the Applicant respectfully submits that Joo and Yamazaki '163, either alone or in combination, do not teach or suggest that a conductive layer extends beyond each periphery of first and second semiconductor layers (a semiconductor layer) at least when selective heating of the first and second semiconductor layers (the semiconductor layer) is performed; or a step of etching the conductive layer after the selective heating of the first and second semiconductor layers (the semiconductor layer) to form at least first and second gate electrodes (a gate electrode) over the first and second semiconductor islands, respectively (the semiconductor layer).

Since Joo and Yamazaki '163 do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

The Official Action rejects dependent claims 18, 23, 75 and 78 as obvious based on the combination of Joo, Yamazaki '163 and U.S. Patent Application Publication No. 2002/0000551 to Yamazaki. Please incorporate the arguments above with respect to the deficiencies in Joo and Yamazaki '163. Yamazaki '551 does not cure the

deficiencies in Joo and Yamazaki '163. The Official Action relies on Yamazaki '551 to allegedly teach the features of the dependent claims. Specifically, the Official Action relies on Yamazaki '551 to allegedly teach a transmittance of 50% of higher with respect to an electromagnetic wave within the wavelength band, forming a first conducting film comprising metal nitride and forming a second conducting film over the first conducting film as a part of the gate electrode (pages 5-6, Paper No. 20070117).

However, Joo and Yamazaki '163 and Yamazaki '551, either alone or in combination, do not teach or suggest the following features or that Joo and Yamazaki '163 should be modified to include any of the following features: that a conductive layer extends beyond each periphery of first and second semiconductor layers (a semiconductor layer) at least when selective heating of the first and second semiconductor layers (the semiconductor layer) is performed; or a step of etching the conductive layer after the selective heating of the first and second semiconductor layers (the semiconductor layer) to form at least first and second gate electrodes (a gate electrode) over the first and second semiconductor islands, respectively (the semiconductor layer).

Since Joo and Yamazaki '163 and Yamazaki '551 do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

New dependent claim 81 has been added to recite additional protection to which the Applicant is entitled. Claim 81 is supported in the present specification, for example, at page 25, lines 17-19. For the reasons stated above and already of record, the Applicant respectfully submits that new claim 81 is in condition for allowance.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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